Introduction

•Modeling and Control of Reentrant Flows: An Intel Sponsored Project

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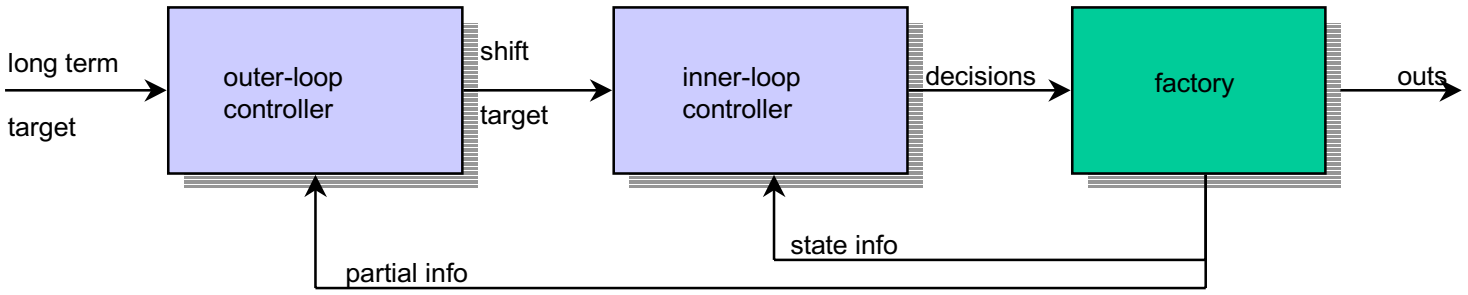
Controlling the Fab

- Resource allocation in the presence of uncertainty
- Resources: Machines, operators, transportation systems
- Uncertainty: Machine failure, repair, processing times, work availability
- Problems: Batching, set-ups, utilization constraints, buffer sizes

Hierarchical Control Design

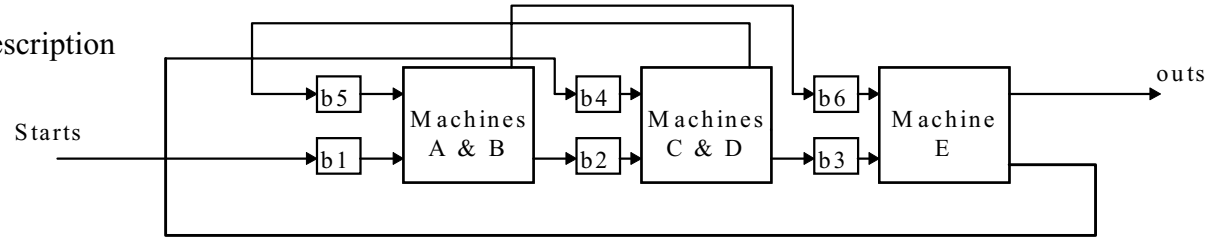
- Time-scale decomposition
  - Low-level (inner-loop): minutes, seconds, discrete-events
  - High-level (outer-loop): Shift, week, average behavior



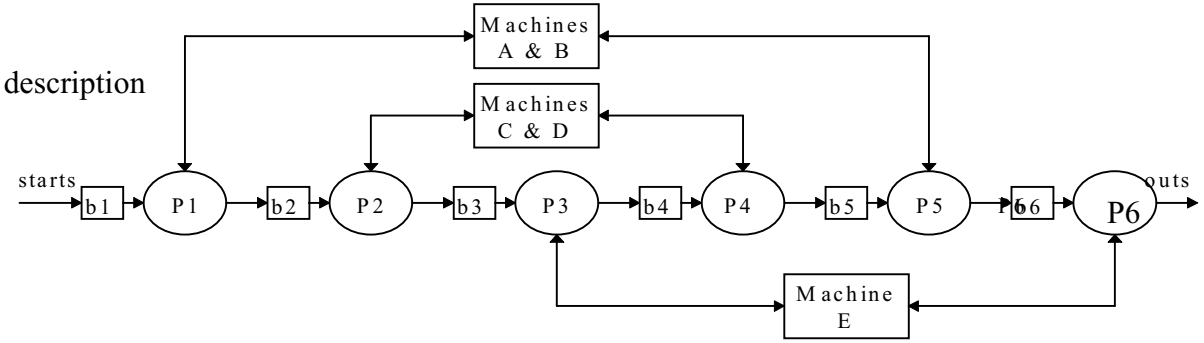
Gershwin, 89

Intel's Mini-Fab

a. Machine-based description



b. Process-based description



	Process time	Process time	Batch size
Machines A & B	Step 1: 225 min.	Step 5: 255 min.	3
Machines C & D	Step 2 30 min.	Step 4 50 min.	1
Machine E*	Step 3 55 min.	Step 6 10 min.	1

* Machine E undergoes set-ups when switching between steps

- Abstraction of a real fab, exposing the key difficulties and limitations of scheduling
- Detailed specs (K. Kempf) include

  Re-entry, Disparate processing times, EM, PM, Operators, Batching, Set-ups, Multiple products

Detailed Spec of the 5-6 Mini-Fab (1)

1. Products and Test-Wafers

P_a starts: 51 lots/week, P_b starts: 30 lots/week, TW starts: 3 lots/week Total: 84 lots/week (~6 lots/shift);
Note: 4 lots/week will be lost due to emergency breakdowns

2. Process Flow

There are 6 processing steps denoted by S_i, i=1…6; they are subject to machine restrictions (batching, setups)

starts >> S_1 >> S_2 >> S_3 >> S_4 >> S_5 >> S_6 >> outs

Note: Only one lot of test wafers may appear in a batch. A test lot cannot run through the same machine twice,
except at a unique machine that runs multiple steps. Test wafers run through the full process,
require setups and can be included in batches.

3. Equipment Set

There are 5 machines denoted by M_i, i=a…e;

M_a = M_b batch 3 lots and serve steps S_1 and S_5 (parallel batching)
M_c = M_d serve steps S_2 and S_4 (variable availability)
M_e serves steps S_3 and S_6 (serial batching/setups)
M_e setup on step change: 10 min
setup on product or test lot change: 5 min
setup on step and product/test lot change: 12 min

Detailed Spec of the Mini-Fab (2)

4. Processing times

S_1 = 225 min; S_2 = 30 min; S_3 = 55 min; S_4 = 50 min; S_5 = 255 min; S_6 = 10 min

Equipment preemption does not occur. Once a machine begins the execution of a step, it must complete it before it starts any other activity. Processing times do not include loading/unloading or setups.

5. Product Mix

Product/test lots waiting for different steps cannot be mixed. S_1 can mix products and one test lots. S_5 cannot mix products but can mix one test lot. M_e setups require a machine and and operator for the setup time. Setups can only be done immediately prior to the execution of the run that the setup is intended to enable.

6. Personnel

There are two production operators (PO_1, PO_2) available for 540 min/shift (1 shift = 12 hours). Each gets two 60 min breaks and one 60 min meeting/training session per shift.

There is one maintenance tech (MT) available for 600 min/shift. MT gets two 45 min breaks and one 30 min meeting/training session per shift.

Personnel preemption does not occur. Once they begin a task, they must complete it before any other task can begin. The off-times need not be synchronized in any way.

Detailed Spec of the Mini-Fab (3)

7. Assist Times

M_a, M_b/S_1,S_5: PO_1 load = 20 min, unload = 40 min
M_c, M_d/S_2,S_4: PO_1 or PO_2 load = 15 min, unload = 15 min
M_e/S_3,S_6: PO_2 load = 10 min, unload = 10 min

Machine runs require PO assist at the beginning (load) and end (unload) of the run but not during processing.
For machines M_c and M_d, the same operator does not have to perform both loading and unloading.

Preventive Maintenance (PM) and Emergency Maintenance (EM): require MT
PM: M_a, M_b: 75 min/day/machine; M_c, M_d: 120 min/shift/machine; M_e: MT 30 min/shift
EM: M_c, M_d: 420 +/- 60 min/machine every 50 +/- 26 hours.

EM requests can only happen while the machine is running. PM window opens at the later of
[beginning-of-shift, last-PM+6 hours], and PM must be completed by end-of-shift.
Or, the later of [beginning-of-day, last-PM+12 hours] and must be completed by end-of-day.

8. Cell Layout and Transportation

S = starts warehouse, buffer = infinite; C_1 = M_a & M_b, max.buffer = 18 lots;
C_2 = M_e, max.buffer = 12 lots; C_3 = M_c & M_d, max.buffer = 12 lots; O = outs warehouse, buffer = infinite

Product Loop: S <> C_1 <> C_2 <> C_3 <> O
Any transportation job takes 4 min; any load/unload transaction takes 1 min; only one lot can be in transport at any one time.
Personnel Loop: C_1 <> C_2 <> C_3 (1 min each transport)

Source: K. Kempf, "Detailed description of a Two-Product, Five-Machine, Six-Step Re-entrant Semiconductor Manufacturing System," *Intel Co. Report,* Technology and Manufacturing Group, Aug. 1994.

Modeling

A Synchronized Fab Model

- Sampling of the discrete event system
- Mass-balance equations at a fast time-scale
- Utilization constraints

$$x_{k+1} = Ax_k + B_1u_k + B_2s_k$$
$$L_0u_k \le L_1 + L_2x_k$$
$$0 \ge f(u_k, x_k)$$

Averaging and the flow model

- Averaging/weighted model reduction yields the flow model

$$x_{kN+N} = A\,x_{kN} + B_1\overline{u}_{kN} + B_2\overline{s}_{kN}$$
$$L_0\overline{u}_{kN} \le L_1 + L_2\,x_{kN}$$

input = sum of inputs over the window (kN, kN+N)

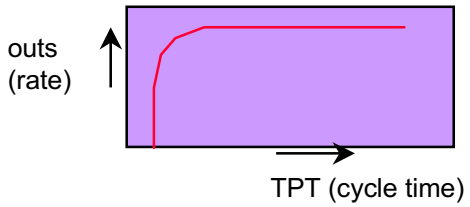
$$\hat{x}_{k+1;N} = A\,\hat{x}_{k;N} + B_1\hat{u}_{k;N} + B_2\hat{s}_{k;N}$$
$$L_0\hat{u}_{k;N} \le L_1 + L_2\hat{x}_{k;N}$$

state/input = average state/input over a rolling window (N)

- Adjustment constraints to capture some of the nonlinear small time-scale constraints

Control Issues

- Objective: More outs, in less time, "nicely" distributed



- Problems: Initial conditions, Batching, Set-ups, EM, PM,…

Control Policies

Low-Level Control Policies

- Low level tracking controllers
  - Via Dynamic Programming (impractical)
  - Use of low-period periodic functions (Kawski)
  - Other simple tracking policies (E.g., assign priorities based on goals or buffers at the beginning of the interval; or, prevent excessive set-ups)

High-Level Control Policies

- Design a controller for the averaged model (linear ODE with constraints)
- Objective: "Optimal" trade-off between Outs and Throughput Time
  - State-Variable feedback (e.g. clear-a-fraction, one-step-ahead, MPC/constrained optimization)
- Release policies (starts) to maximize outs
  - MPC (Rivera), State-constraints (Rodriguez)

A Simple Scheduling Example (Intel's Mini-Fab)

- Tracking inner loop, Constrained minimization (one-step ahead) outer-loop.
- Convergence (can be predicted by the flow model with an "appropriate" adjustment of the constraints)
- Role of set-ups and batching (loop "instability" for policies leading to excessive set-ups -FIFO, LBFS)
- Effect of initial conditions, quantization (multiple steady-states)

Simulation Results

Buffer convergence and comparisons with the closed-loop flow model

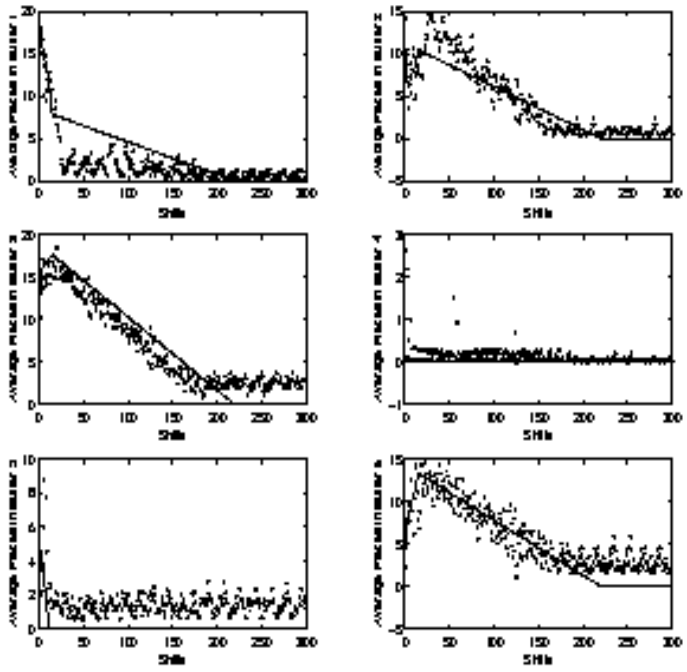


Figure 8: Average buffer sizes for the closed loop flow model (solid line) and the closed loop "simulator" (dots). Starts release rate of 6.18 pieces per shift.

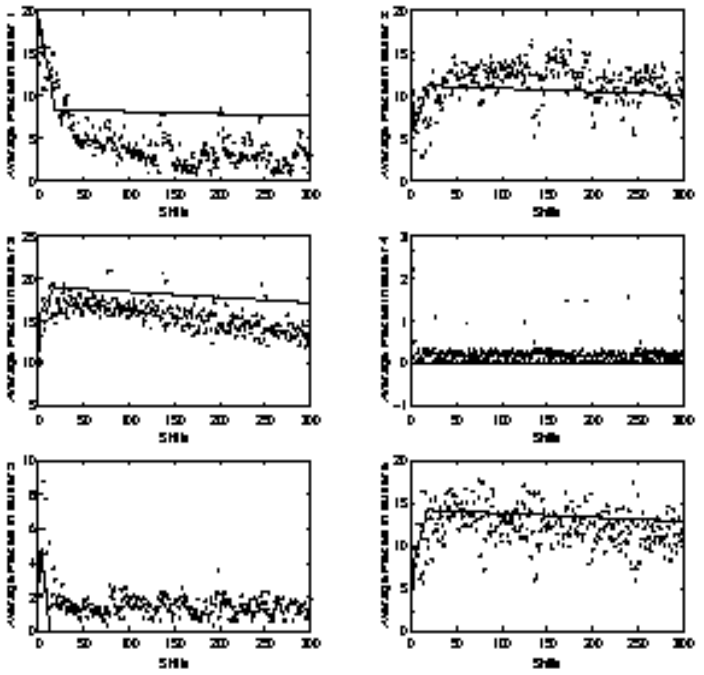


Figure 9: Average buffer sizes for the closed loop flow model (solid line) and the closed loop "simulator" (dots). Starts release rate of 6.36 pieces per shift.

Simulation Results (2)

Plain pull policy with starts release rate of 6.36 parts/shift. Buffer instability caused by excessive set-ups

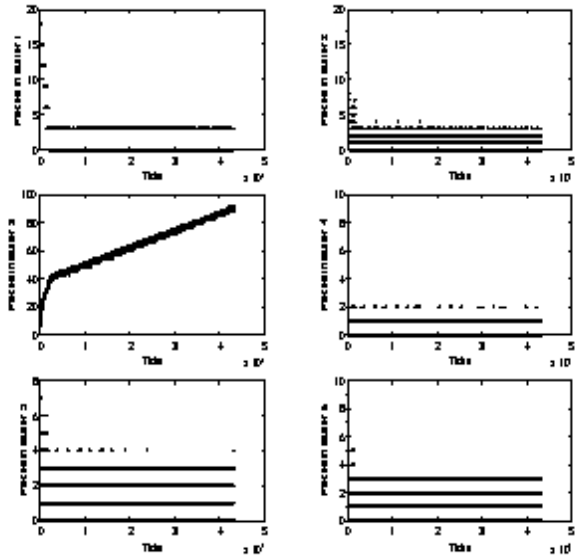


Figure 7: Buffer sizes foa a simple pull policy with start release rate of 6.36 parts per shift.

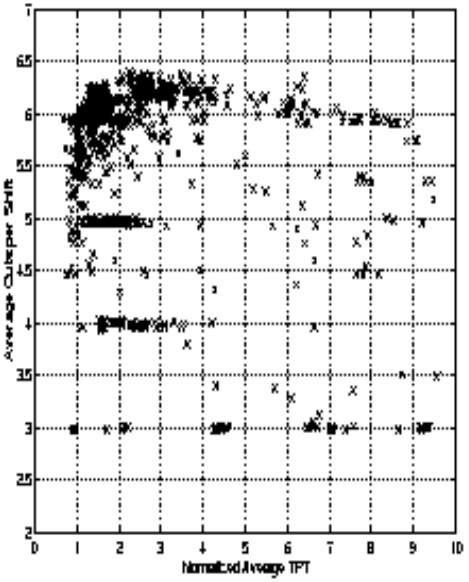


Figure 1: "Intel-like" policies, 2500 different

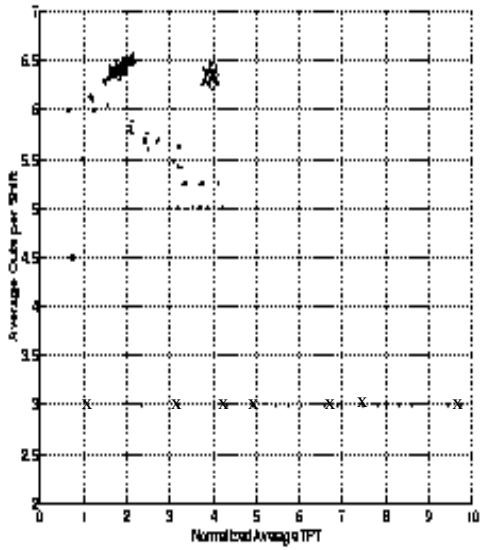


Figure 2: "Intel-like" policies. 10 different "controllers", 44 different initial conditions.

- Exploring the boundary of steady-state performance in the absence of stochastic perturbations (EM, stochastic release, etc.) (see Kawski for analytical computations of the theoretical limits of performance).
- Various Intel-based policies; initial conditions may have significant effect on the steady-state performance (outs and cycle-time)

Simulation Results (3)

Exploring inner-outer, hierarchical controller designs.

- Tracking policies (fixed starts rate)
- Pull-based tracking inner loop
- One-step ahead constrained minimization outer loop

- Maintains steady-state performance "close" to the boundary but exhibits undesirable sensitivity to initial conditions for some release rates. (These patterns often collapse when stochastic perturbations are present)

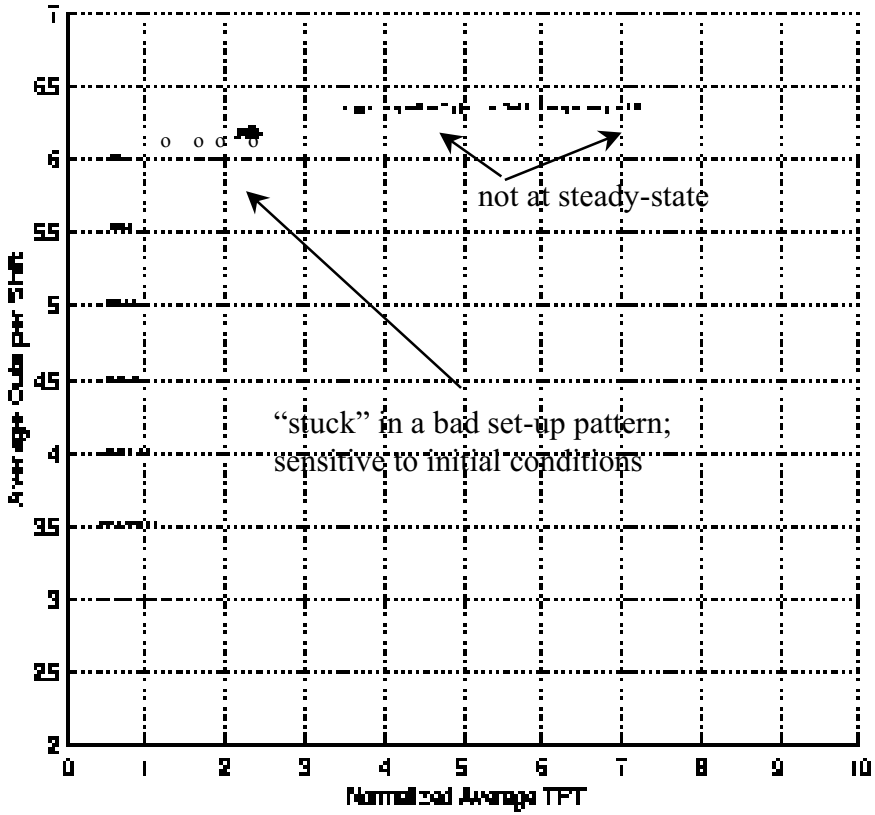


Figure 3: Lyapunov based one step ahead minimization for outer loop, fixed priority inner loop policie, 44 different initial conditions.

Simulation Results (4)

First attempt to remedy the sensitivity to initial conditions

- Variable priority tracking inner loop
- One-step ahead constrained minimization outer loop

- Maintains steady-state performance "close" to the boundary without excessive sensitivity to initial conditions However, the outputs show some (perhaps necessary) irregularity in their distributions

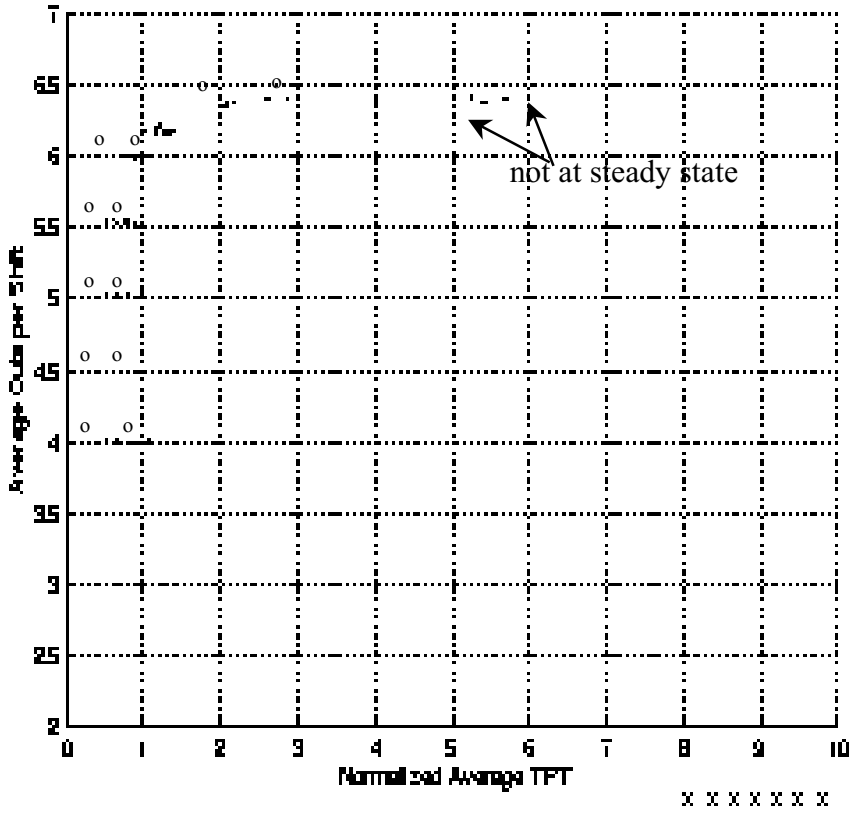


Figure 5: Lyapunov based one step ahead minimization for outer loop, variable priority inner loop policie, 9 different initial conditions.